What is claimed is:

1. An integrated circuit field effect transistor having an amorphous carburized silicon layer gate insulator.

2. An integrated circuit field effect transistor comprising:

a source and a drain separated by a channel supported by a semiconductor substrate;

a gate supported by the substrate and extending between the source and drain above the channel; and

an insulative amorphous layer of carburized silicon formed between the channel and the gate.

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3. An integrated circuit memory device supported by a semiconductor substrate, the device comprising:

a source and a drain separated by a channel supported by a semiconductor substrate;

a floating gate supported by the substrate and extending between the source and drain above the channel;

a control gate formed adjacent to and insulated from the floating gate; and

an insulative layer of carburized silicon formed between the channel and the gate.

4. An integrated circuit capacitor supported by a semiconductor substrate, the capacitor comprising:

a first conductor layer supported by the substrate;

a dielectric layer of carburized silicon formed on top of the first conductor layer; and

a second conductor layer formed on top of the dielectric layer.

5. The capacitor of claim 4 wherein at least part of the layers extend substantially vertically from a general surface of the substrate.

6. The capacitor of claim 4 wherein the capacitor is part of a memory cell, and the layers are formed at least partially over memory cell access circuitry.

7. A memory device comprising:

an array of memory cells having capacitors that store charges representative of data and have access transistors formed with carburized silicon gate insulators;

decode circuitry coupled to the array; and

control circuitry coupled to the decode circuitry and the array of memory cells.

8. A semiconductor memory device comprising:

a memory array including a plurality of transistors, each of the transistors including a source region, a drain region, a conductive channel separating the source and drain regions, and an electrically isolated floating gate located adjacent the channel and separated therefrom by a layer of carburized silicon insulating material, and a control gate located proximal to the floating gate and separated therefrom by a layer of insulating material;

addressing circuitry for addressing the memory array; and

control circuitry for controlling read, write, and erase operations of the memory device.

9. An imaging device comprising:

an array of light sensitive carburized silicon floating gate transistors that store charges on the floating gate and discharge responsive to light;

decode circuitry coupled to the array; and

control circuitry coupled to the decode circuitry and the array of floating gate transistors.

10. A method of forming a gate insulator for a semiconductor device comprising the steps of:

cleaning a silicon substrate;

growing a layer of SiC in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing environment.

11. A method of forming a gate insulator for a semiconductor device comprising the steps of:

growing a first layer of SiC in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrogen and hydrocarbon gas which contains from about 1 to 10 carbon atoms per molecule;

forming the gate on top of the SiC layer; and

forming a source and drain.

12. The method of claim 11 wherein the hydrocarbon gas comprises at least one of methane, ethane, ethylene, acetylene, and ethanol.

13. The method of claim 11 wherein the concentration of hydrocarbon gas in hydrogen is between approximately 2% to 10%.

14. The method of claim 11 wherein the layer of SiC is grown in a pressure of between approximately 15 to 25 Torr.

15. The method of claim 11 and further comprising the step of forming a second SiC layer by chemical vapor deposition of amorphous SiC after growing the first layer and prior to forming the gate.

16. The method of claim 11 wherein a microwave power of between approximately 250 to 1000 watts is used while growing the first SiC layer.

17. A method of forming a gate insulator for a semiconductor device comprising the steps of:

growing a first layer of SiC in a microwave-plasma-enhanced chemical vapor deposition chamber in a 2 to 10% concentration of a hydrocarbon gas which contains from about 1 to 10 carbon atoms per molecule in hydrogen at a pressure of between approximately 15 to 25 Torr;

forming the gate on top of the SiC layer; and

forming a source and drain.

18. A method of forming a gate insulator for a semiconductor device comprising the steps of:

growing a first layer of SiC in a microwave-plasma-enhanced chemical vapor deposition chamber at a microwave power of between approximately 250 to 1000 watts in a hydrocarbon gas which contains from about 1 to 10 carbon atoms per molecule in hydrogen;

forming the gate on top of the SiC layer;

forming a source and drain; and

growing a second SiC layer by chemical vapor deposition of amorphous SiC after growing the first layer and prior to forming the gate.

19. A method of forming a gate insulator for a semiconductor device comprising the steps of:

growing a first layer of SiC in a microwave-plasma-enhanced chemical vapor deposition chamber at a microwave power of between approximately 250 to 1000 watts in a 2 to 10% concentration of a hydrocarbon gas which

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contains from about 1 to 10 carbon atoms per molecule in hydrogen at a pressure of between approximately 15 to 25 Torr;

forming the gate on top of the SiC layer;

forming a source and drain; and

growing a second SiC layer by chemical vapor deposition of amorphous SiC after growing the first layer and prior to forming the gate.